Paper 28.7 – ISSCC2005

A 3Gb/s AC Coupled Chip-to-Chip Communication using a Low Swing Pulse Receiver

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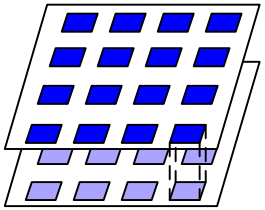
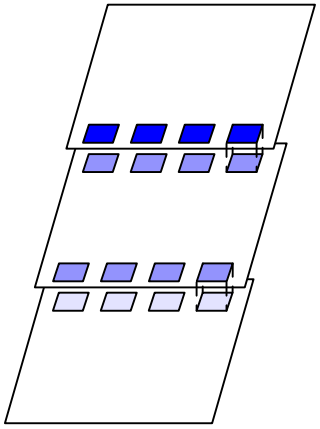
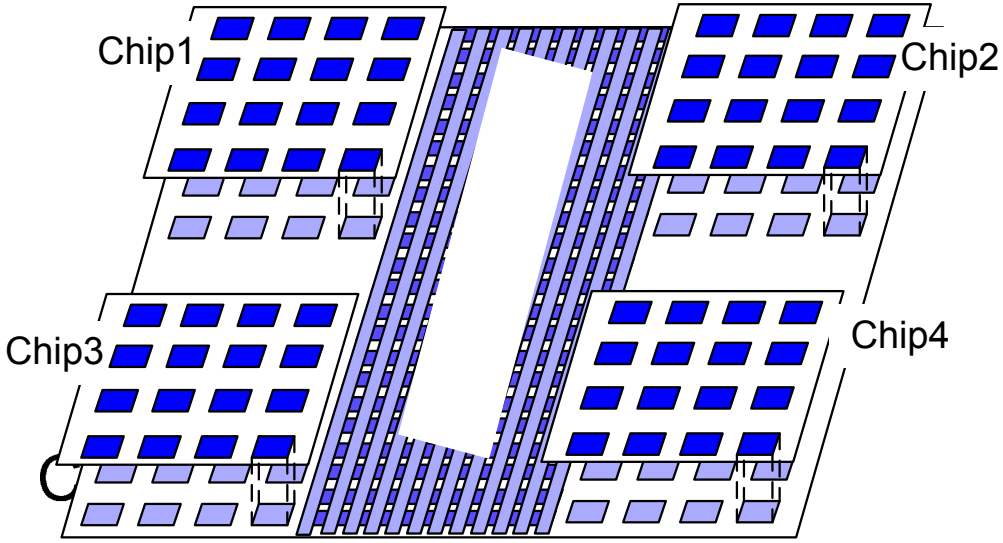
High density Capacitively Coupled I/Os



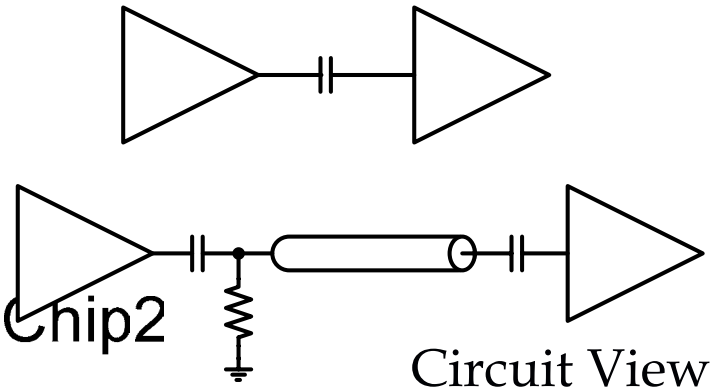
3D-IC



Proximity Comm.



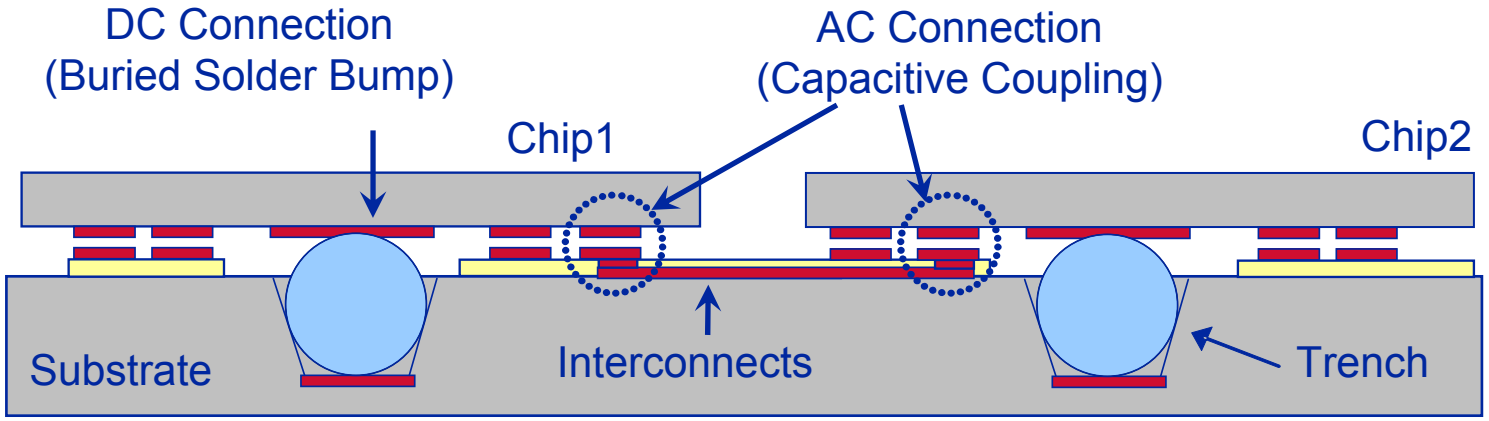
AC Coupled Interconnect



Circuit View

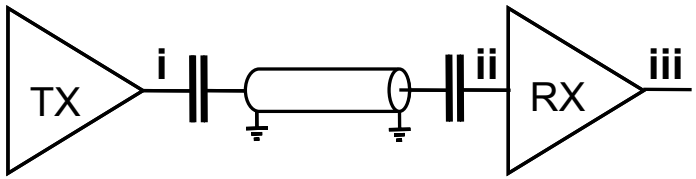
- Density
- Flexibility
- More integration
- Longer Distance
- Lossy

AC Coupled Interconnect (ACCI)

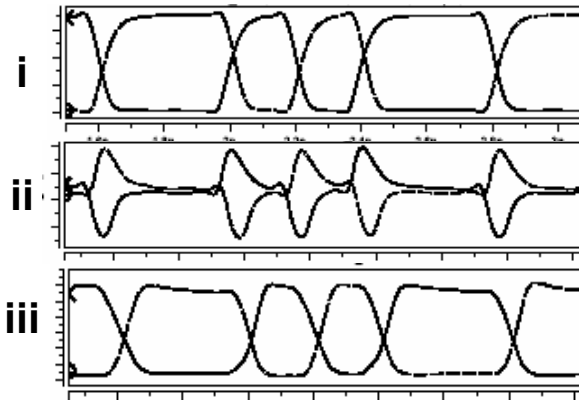


physical structure

75um I/O pitch
6,000+ I/Os /cm^2
Low power

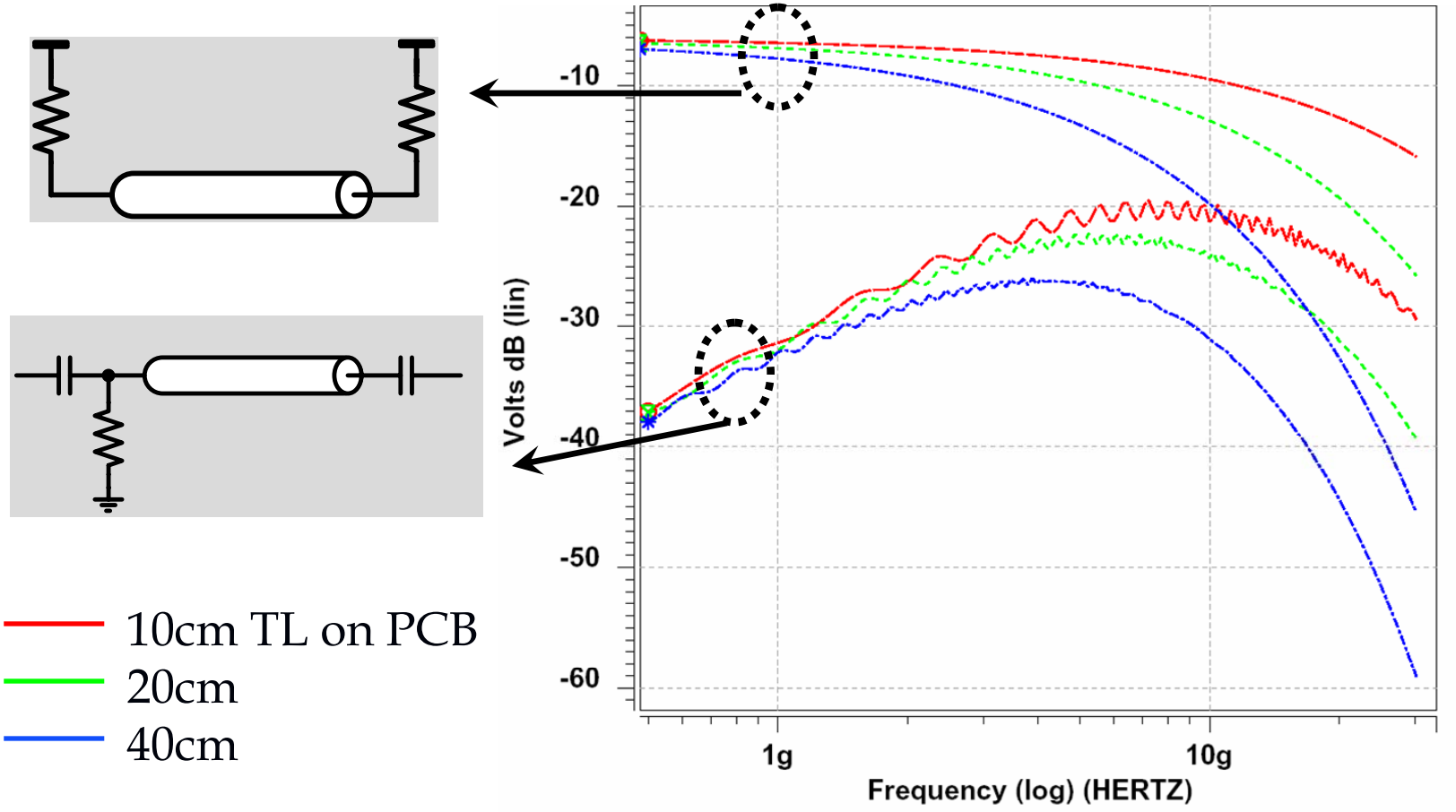


circuit view

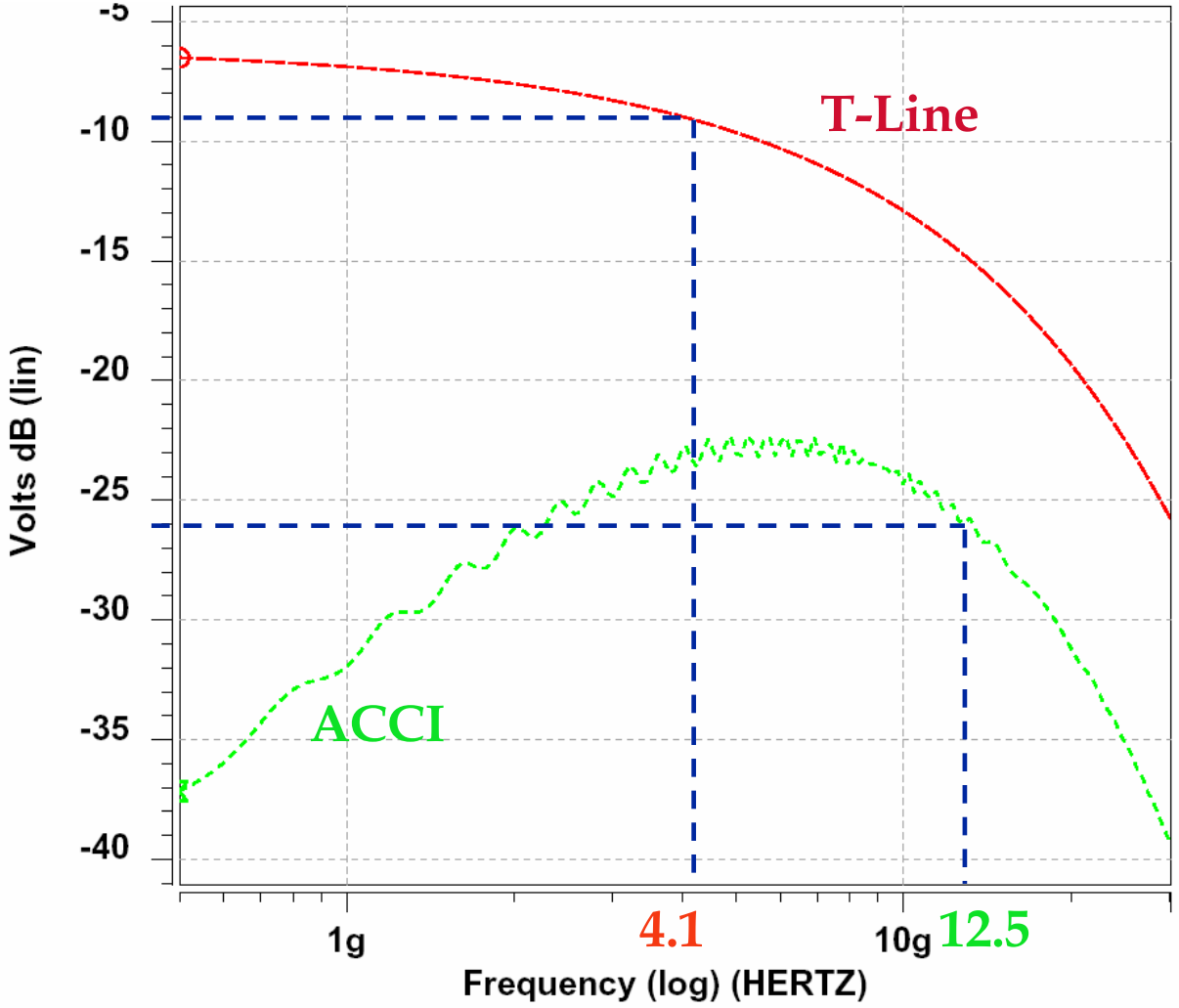


pulse signaling waveforms

Channel Response



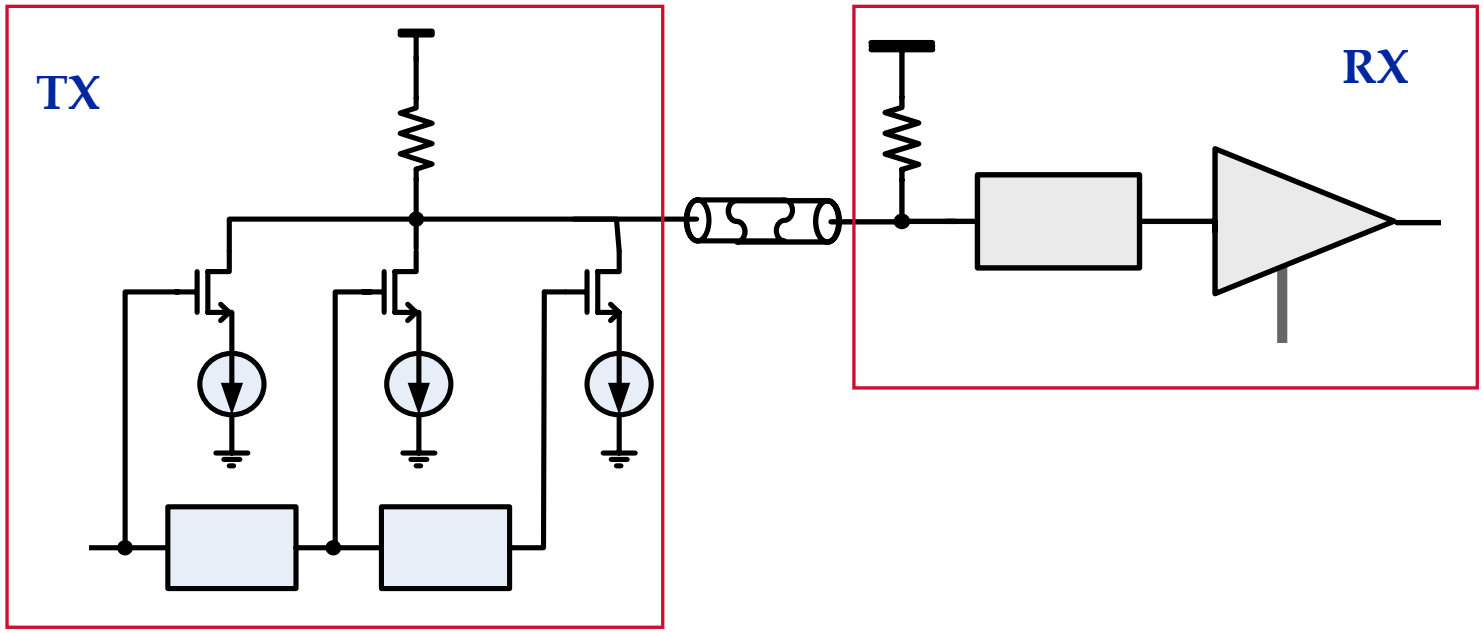
Expand 3dB bandwidth

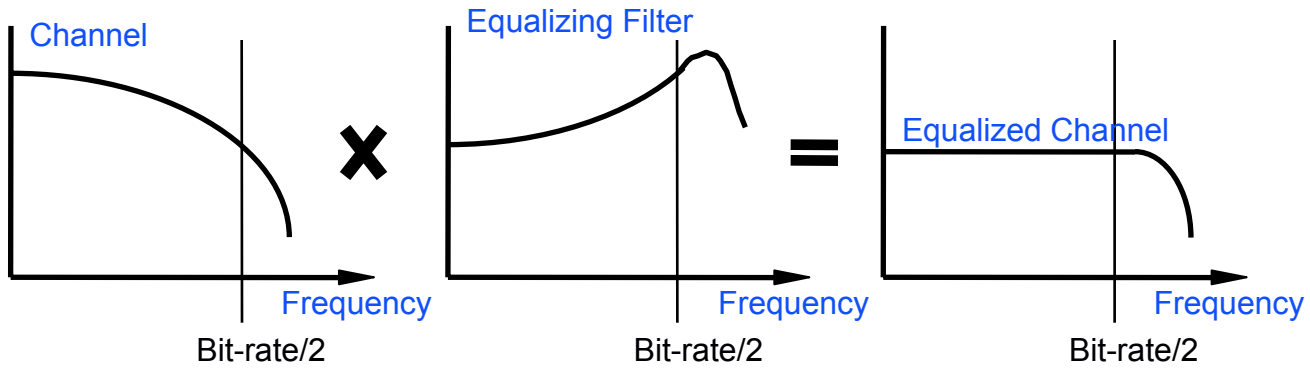


20cm PCB

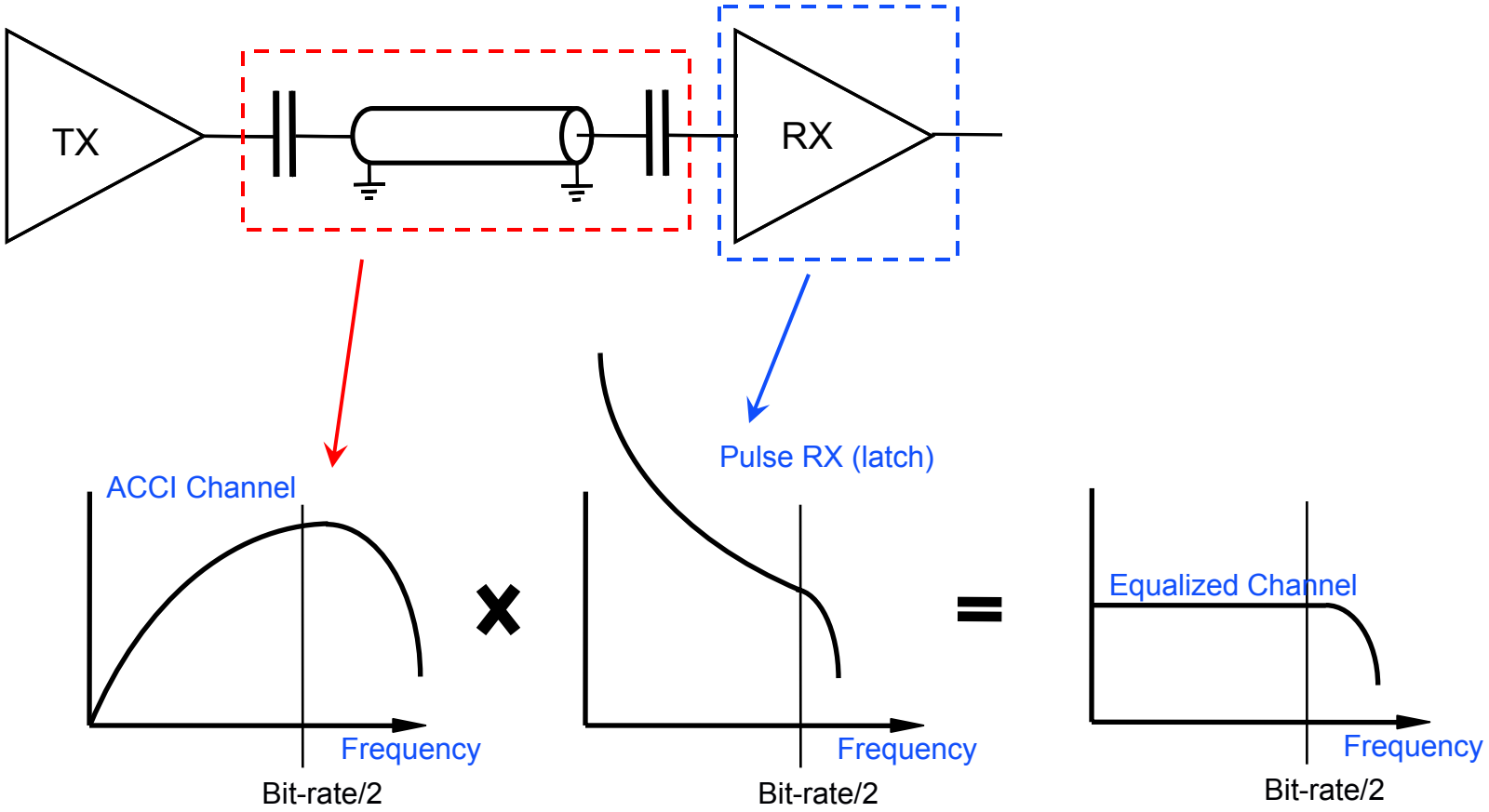
Micro-strip Line

Traditional Equalization

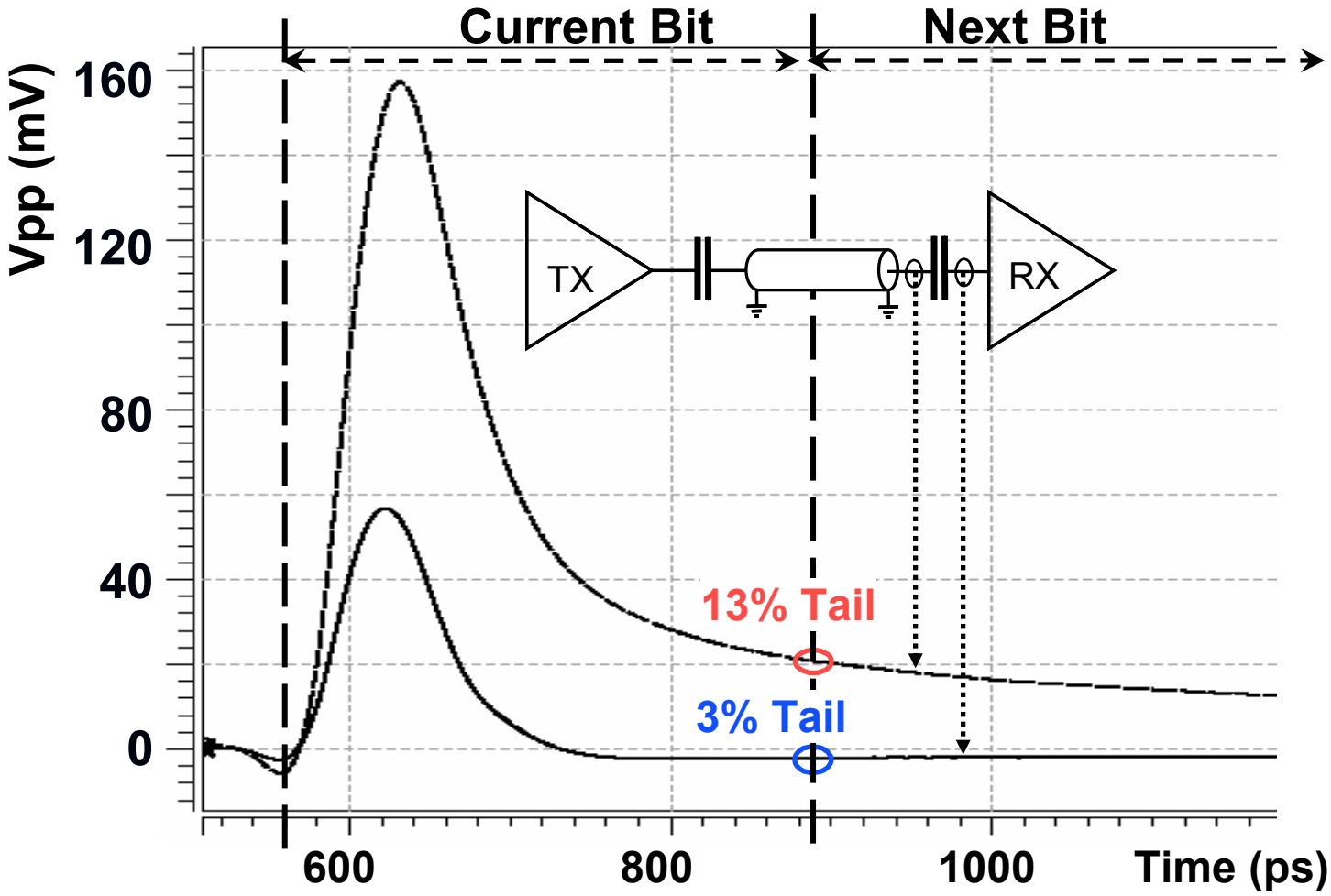




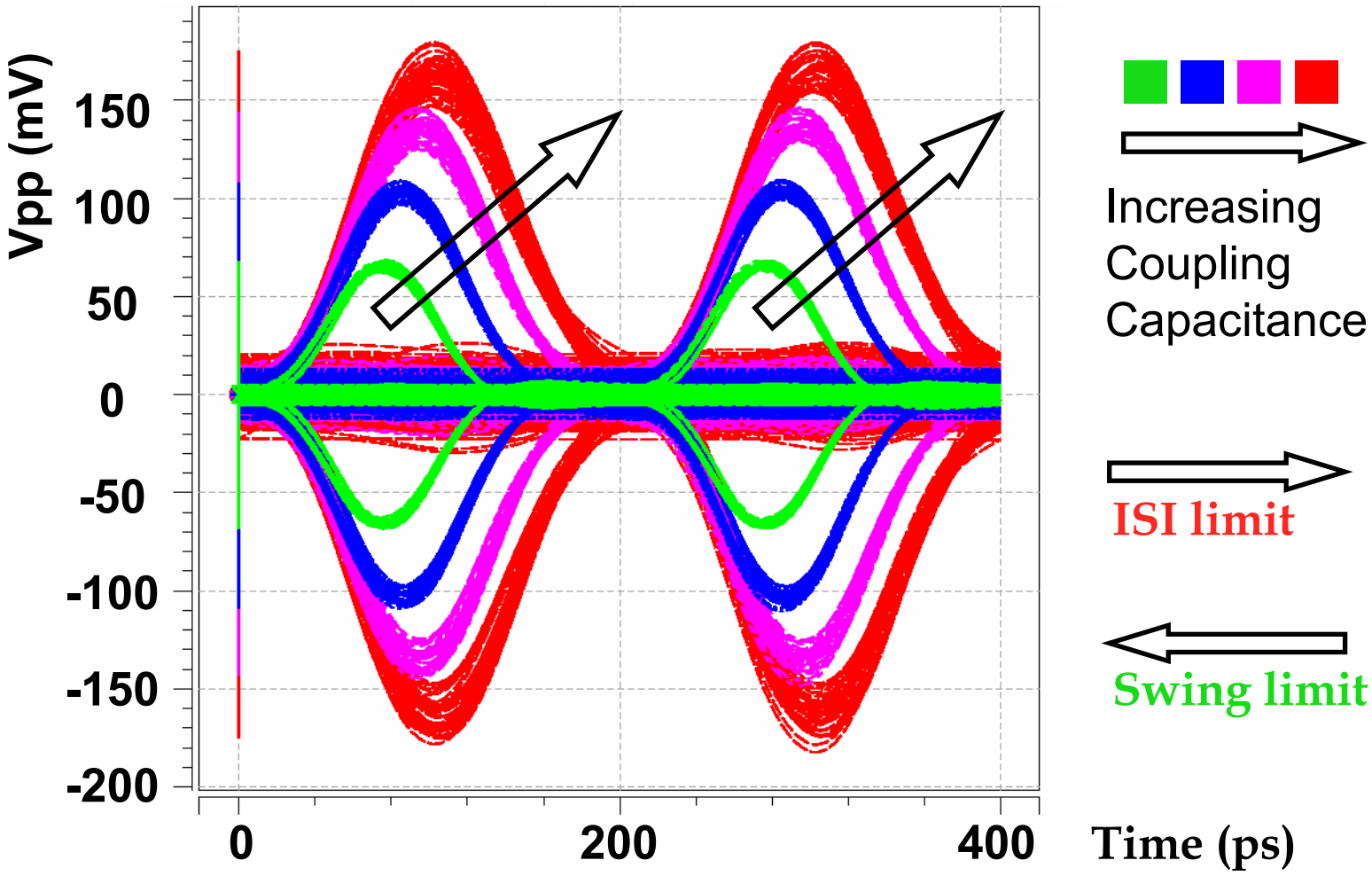
ACCI Equalization



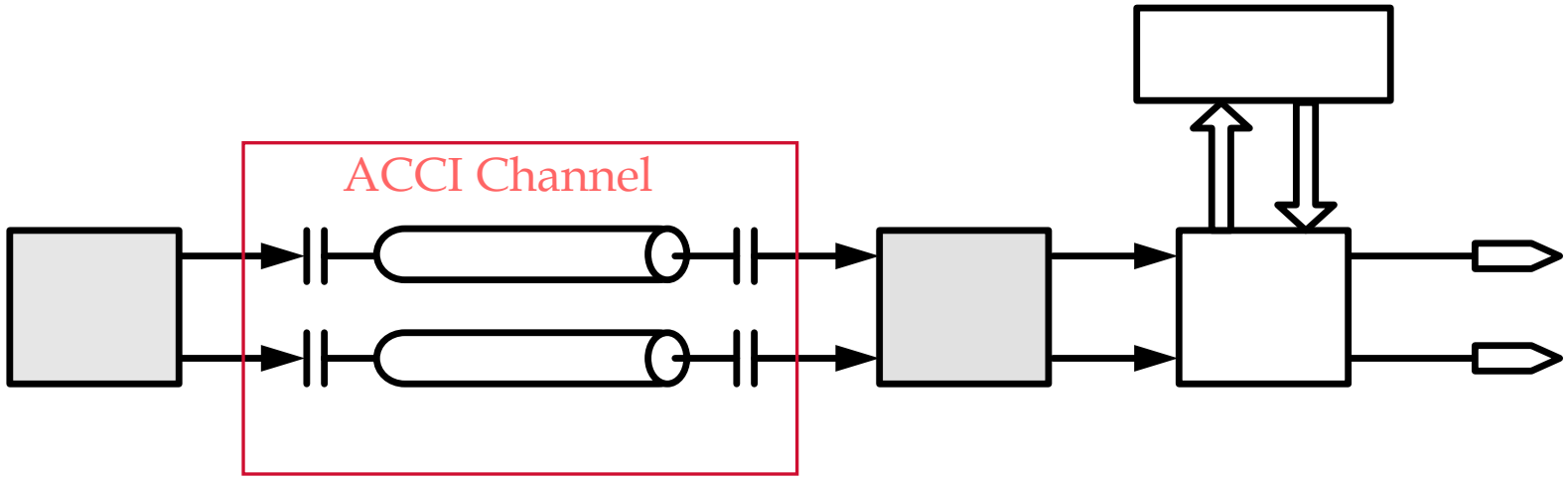
ISI of Pulse Signal



EYE at RX input



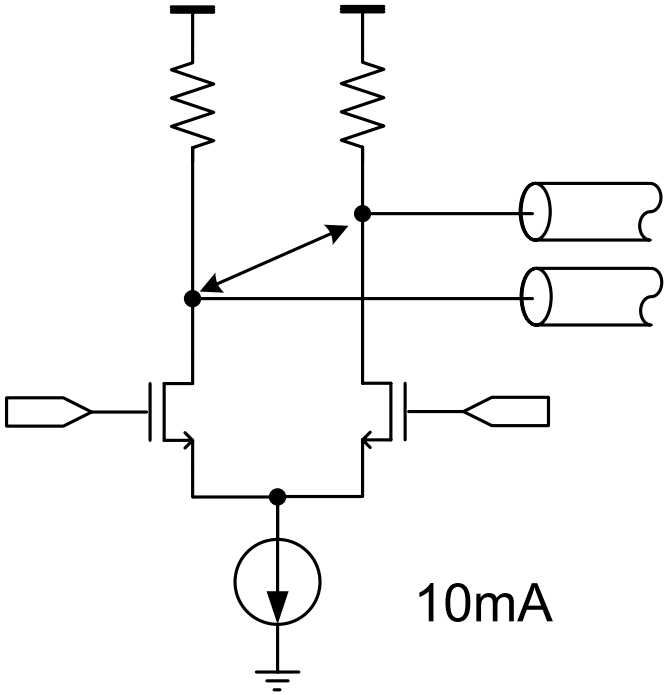
Components of ACCI

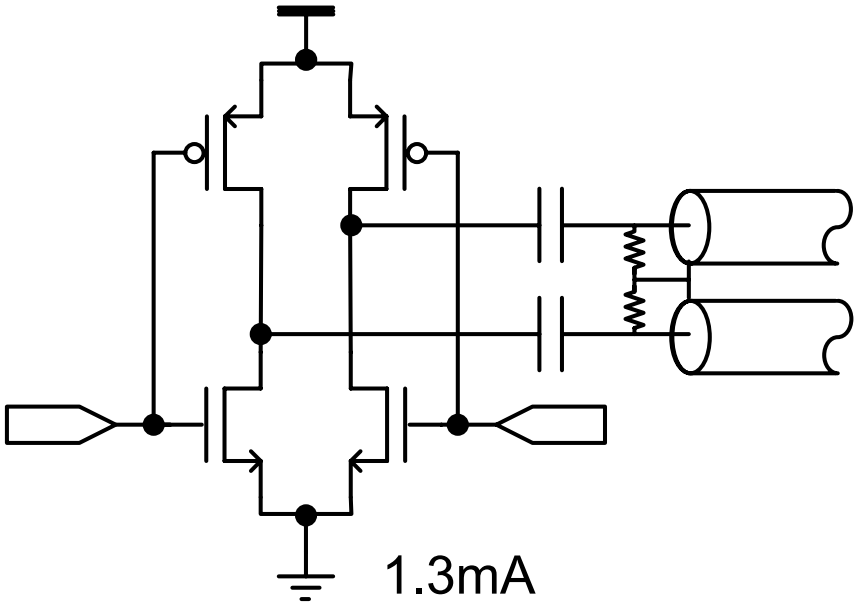


- TX outputs NRZ to channel
- Pulse RX converts pulses back to NRZ, then goes to clock and data recovery

TX

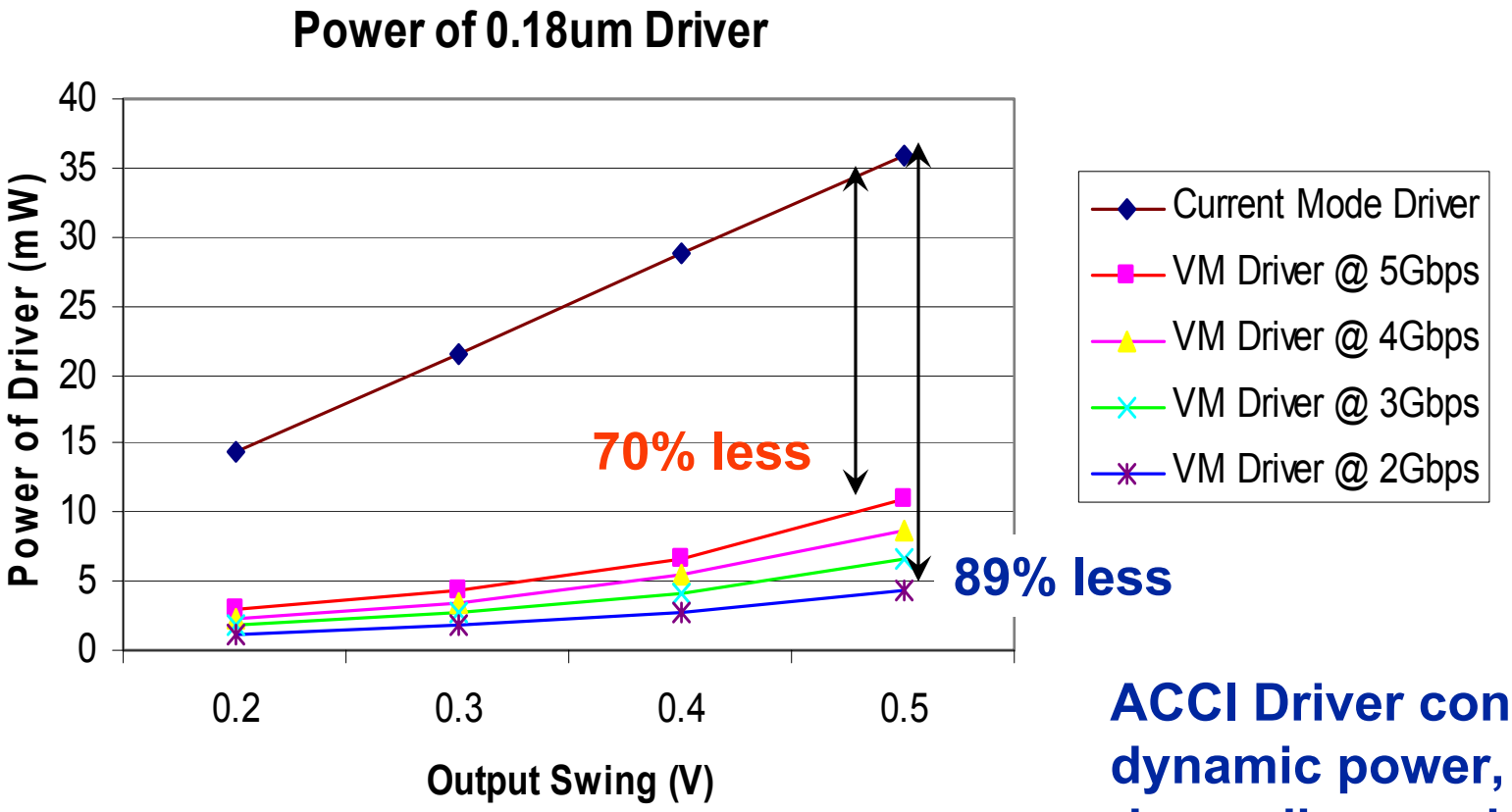
Low power driver





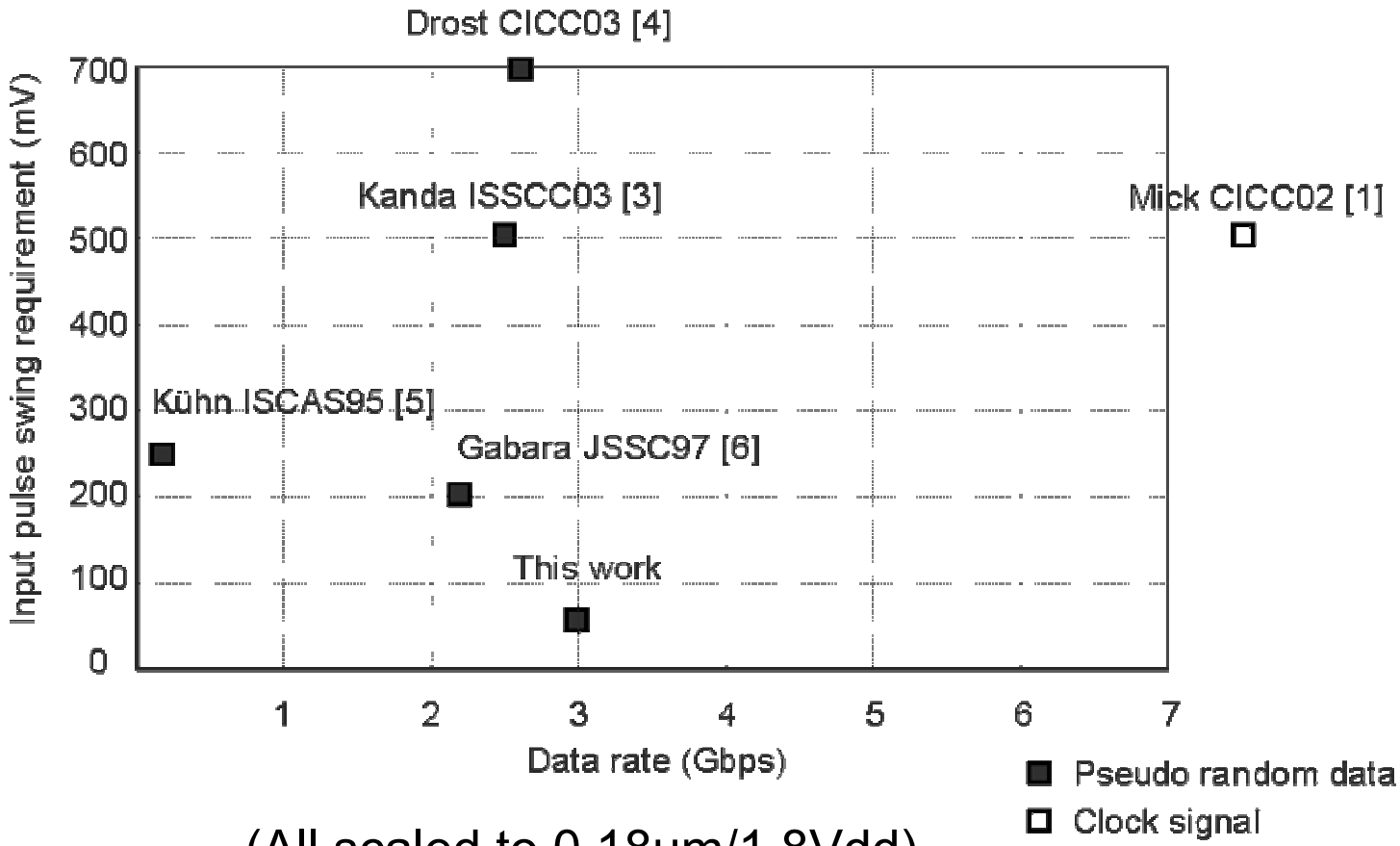
- **Current Mode Vs. Voltage Mode**
  - 50 ohm TL load Vs. Cap load
  - Static current Vs. dynamic current
  - 10mA Vs 1.3mA (to get a $0.25V_{SEPP}$ output swing, for 0.18um CMOS)

Power Saving



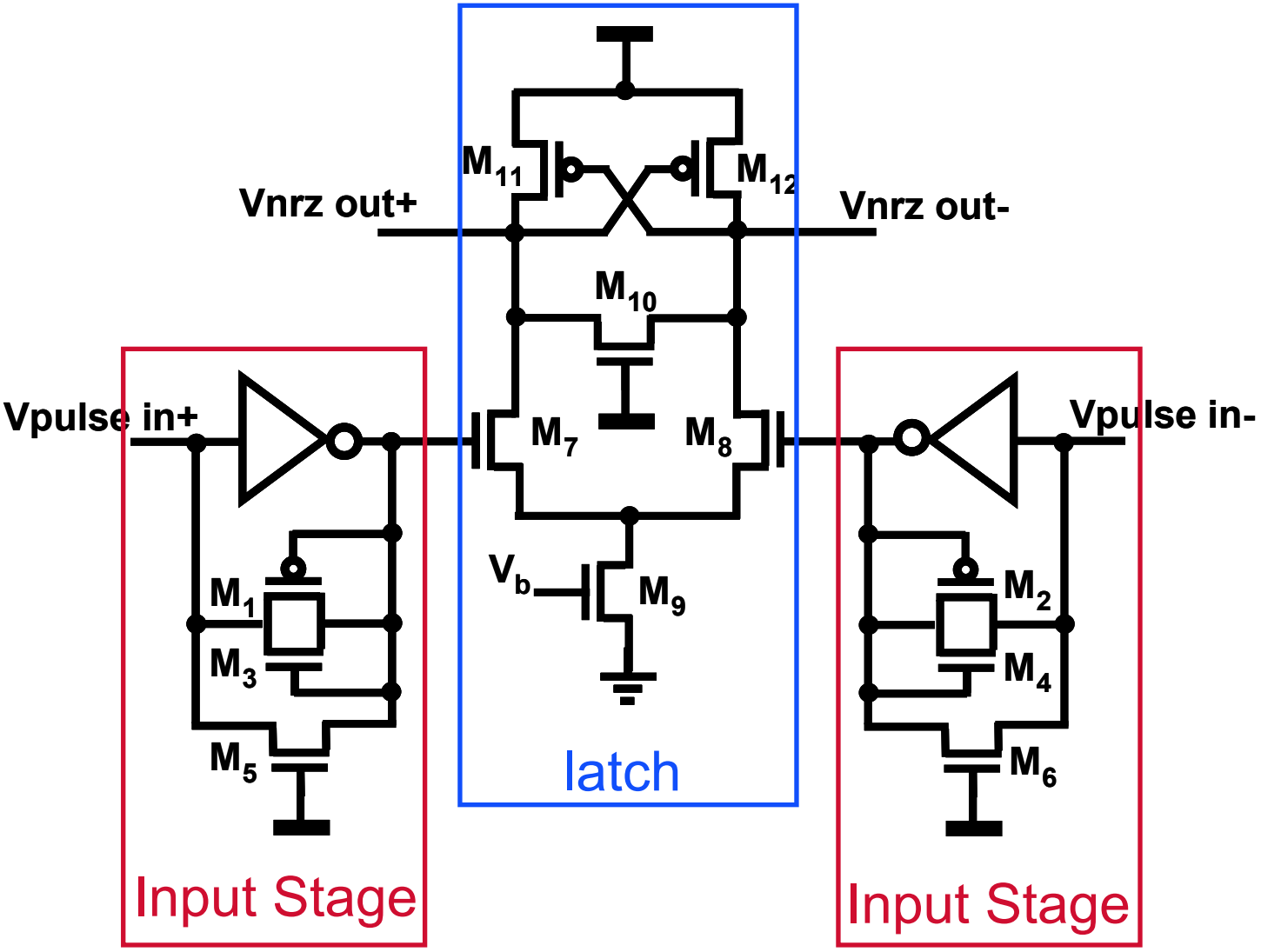
ACCI Driver consumes dynamic power, depending on data rate and data activity

ACCI need sensitive pulse receiver

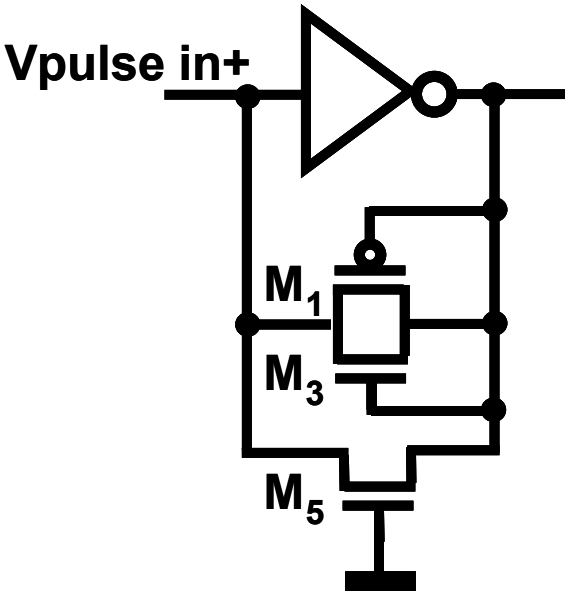


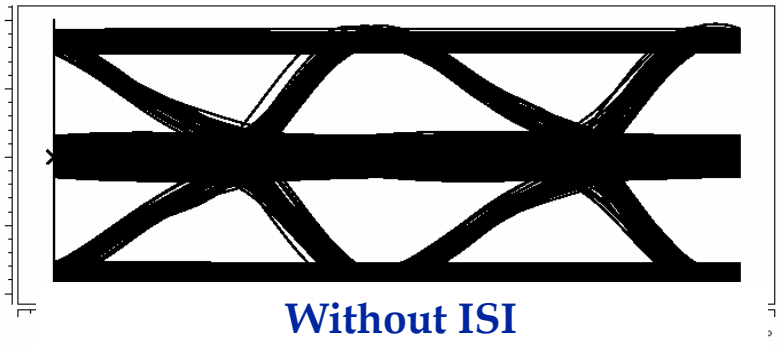
(All scaled to 0.18um/1.8Vdd).

A low swing pulse receiver

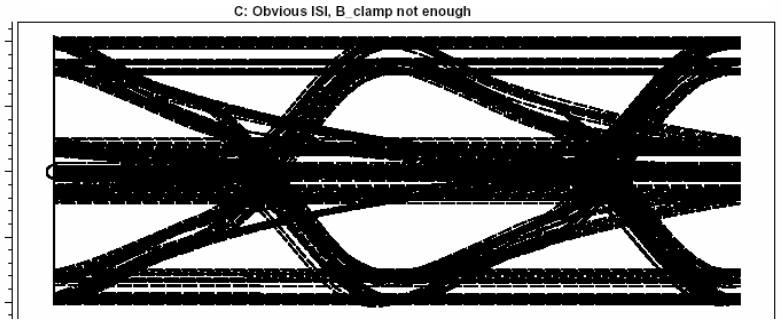


Input stage





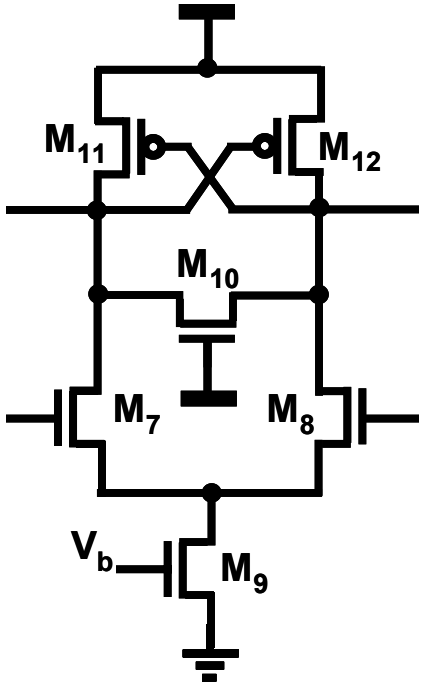
Without ISI

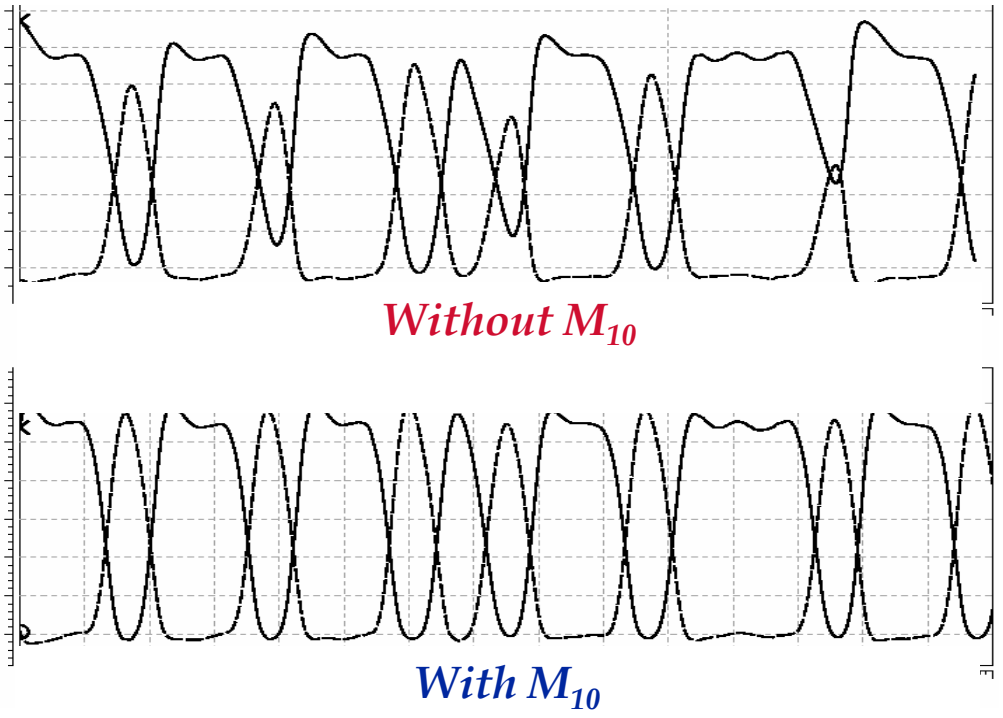


With ISI

- ISI due to limited bandwidth
- Swing Vs. bandwidth tradeoff ➔ INV and feedback ratio

Latch stage

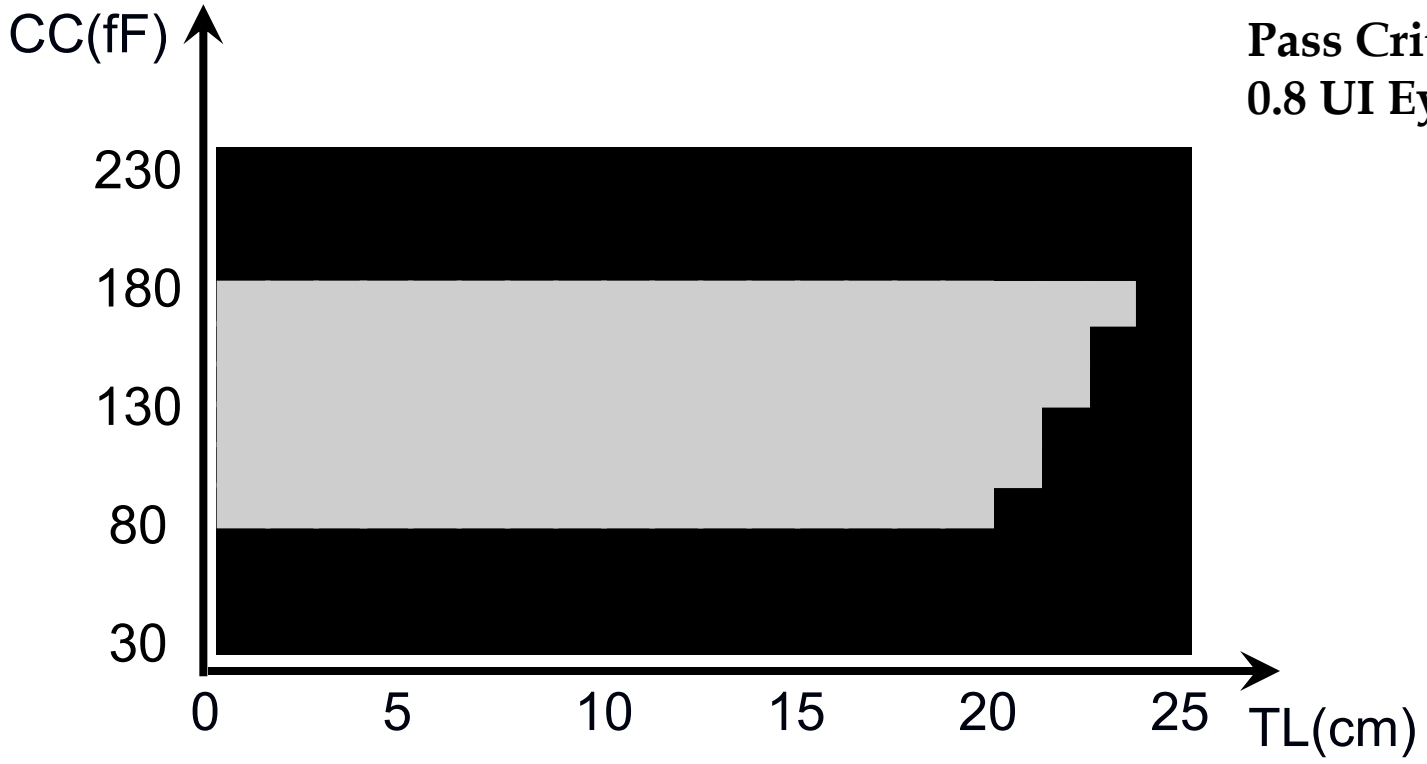




- Latch : M11 and M12; Edge Detector: M7 and M8
- Swing and bandwidth tradeoff ➔ M_{10}

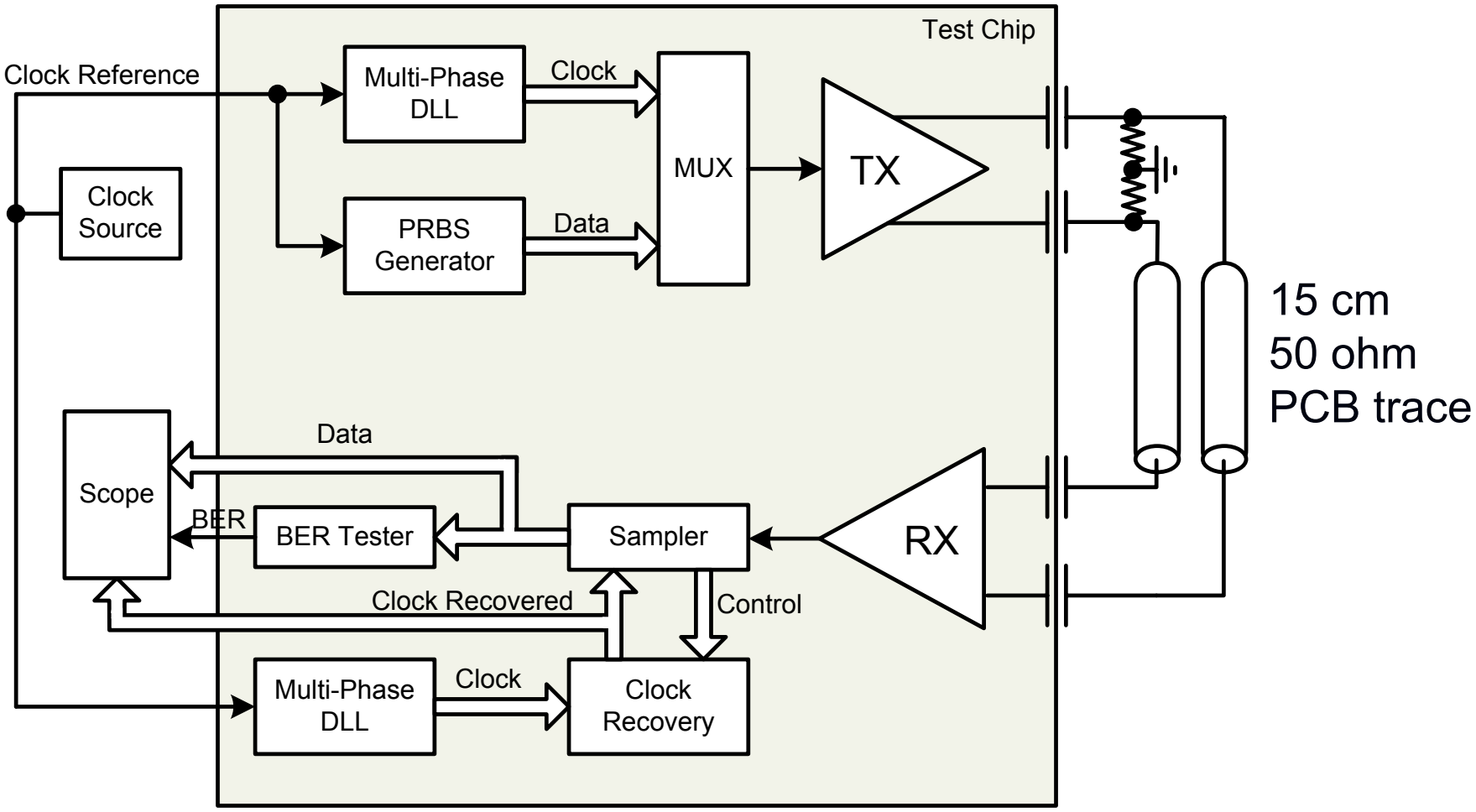
Simulated Shmoo Plot

- **Works over wide range of Coupling Capacitance, TL Length, up to 3Gb/s**

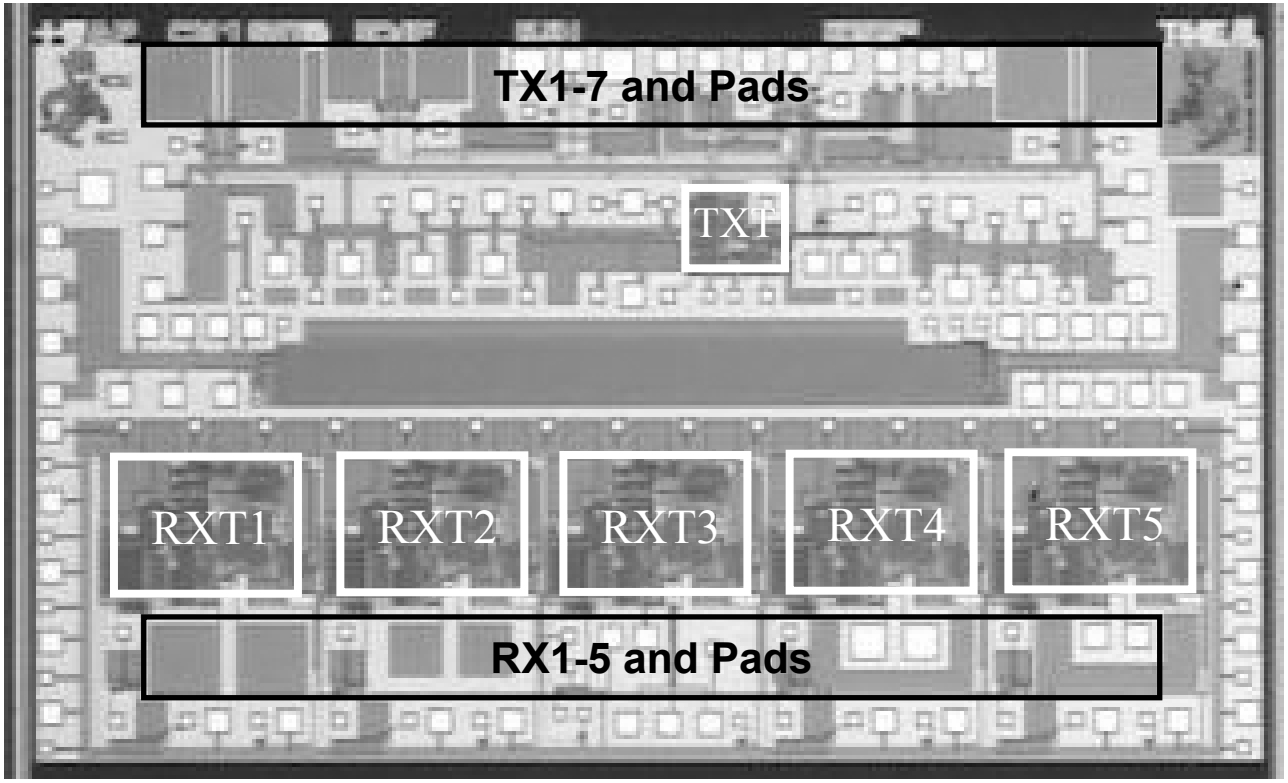


Pass Criteria:
0.8 UI Eye Opening

Test chip

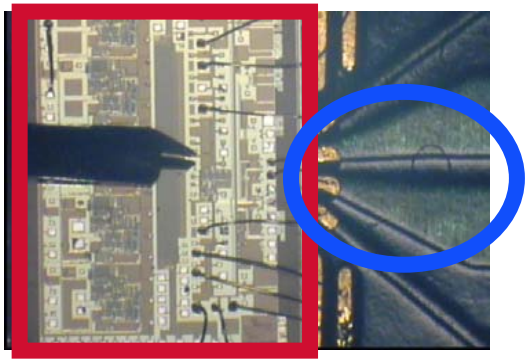

Test Chip
Clock Reference
Multi-Phase DLL
Clock
MUX
TX
Clock Source
PRBS Generator
Data
15 cm
50 ohm
PCB trace
Data
Scope
BER
BER Tester
Sampler
RX
Clock Recovered
Control
Multi-Phase DLL
Clock
Clock Recovery

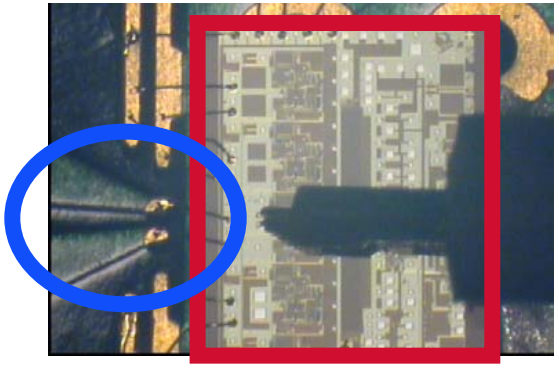
Die photo

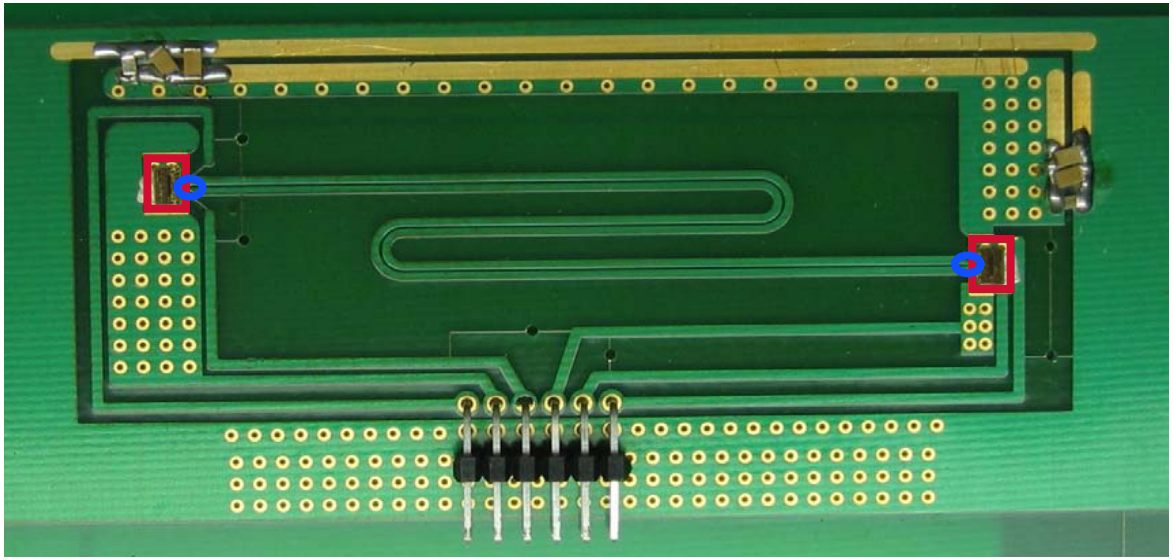


TSMC 0.18um CMOS, 2mm by 3.5mm

Test Setup on PCB







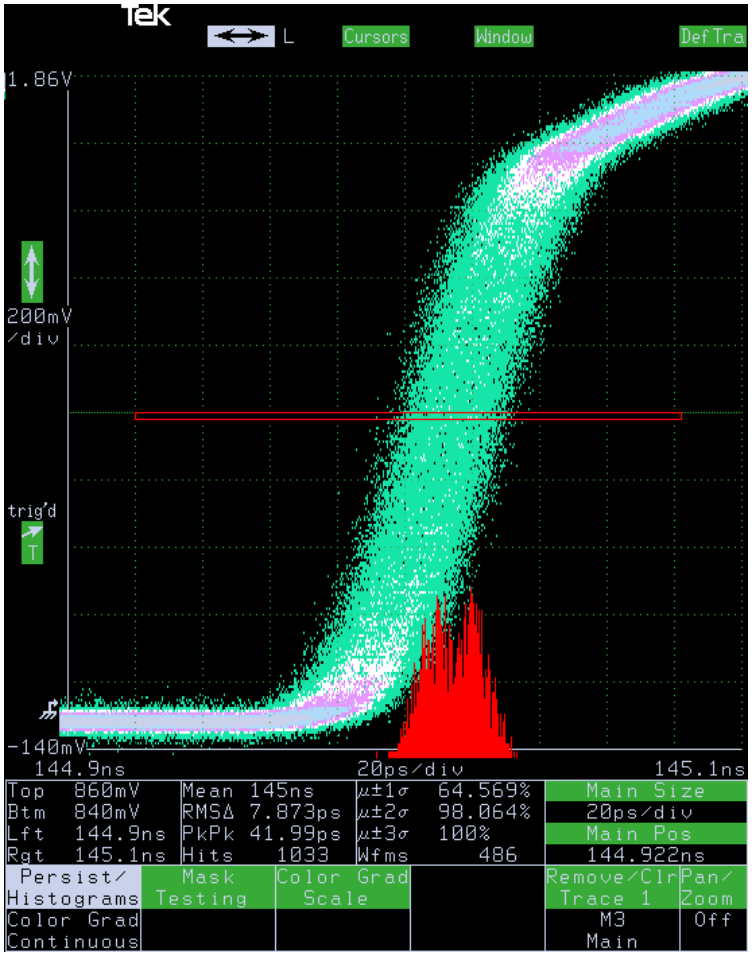
15 cm long 50 ohm differential PCB trace

150fF Coupling Capacitors

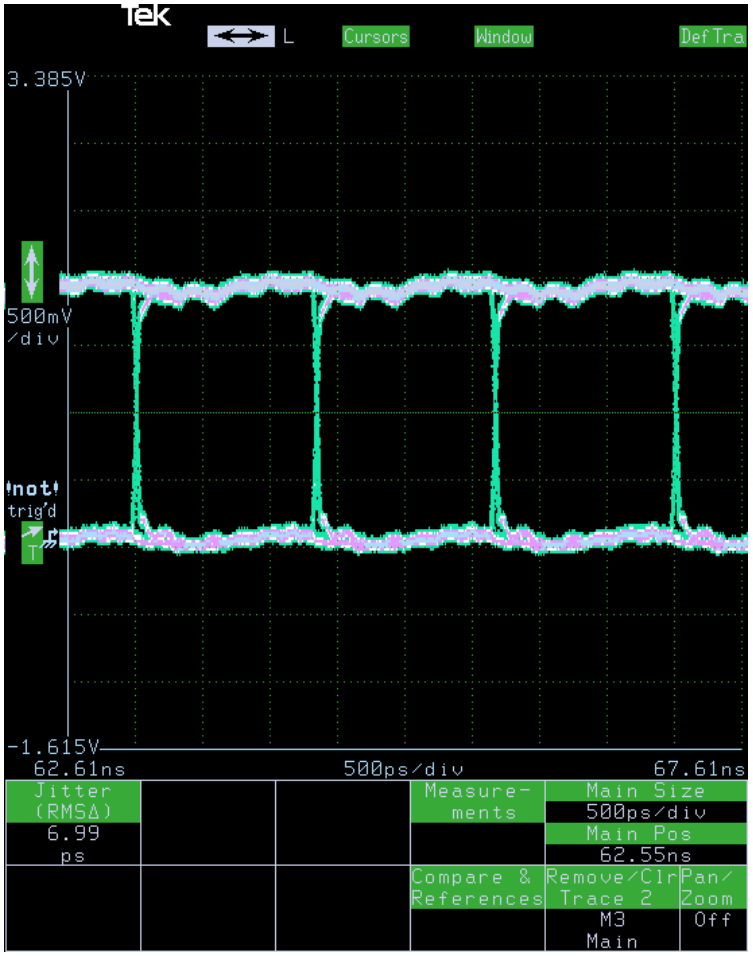
Chip and Measured data

Process		TSMC 0.18um CMOS 1P 6M
Supply Voltage		1.8V
Data Rate		3Gb/s/channel
BER		$< 10^{-12}$
Coupling Caps		60um by 60um on-chip (150fF)
Link		15cm and 50ohm micro-strip line
Jitter of recover data		7ps RMS
Power (mW)	Driver	5
	Pulse RX	10
	Clock, test circuit and buffers	116.5
	Total	134

Recovered Clock and Data



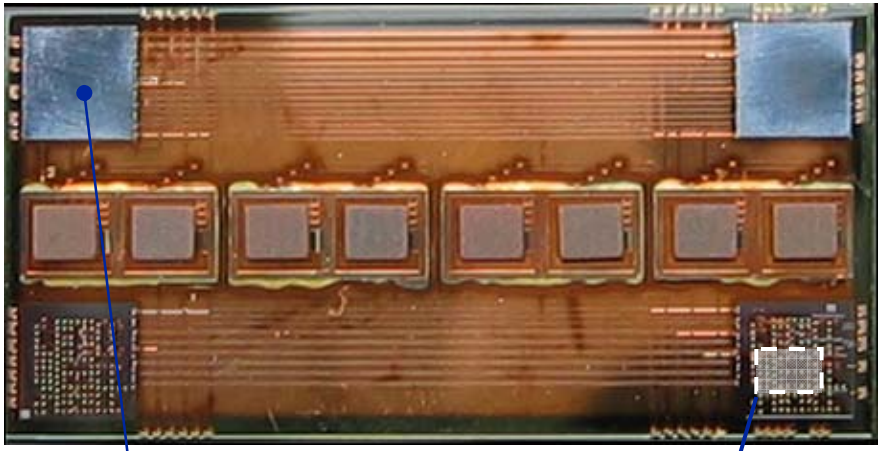
Recovered Clock



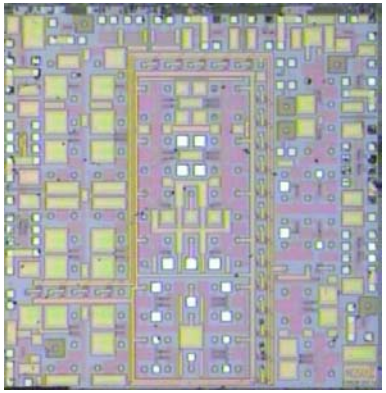
Recovered and Deserialized Data

MCM-D Test

Assembled ACCI System

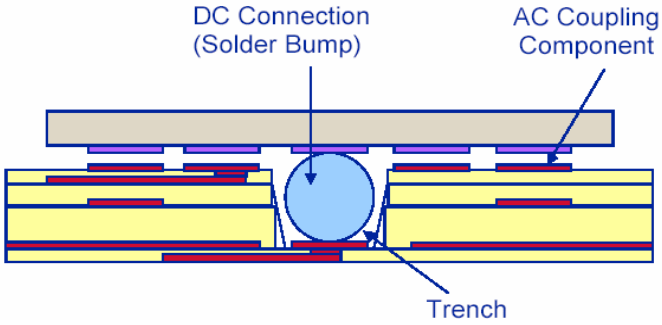


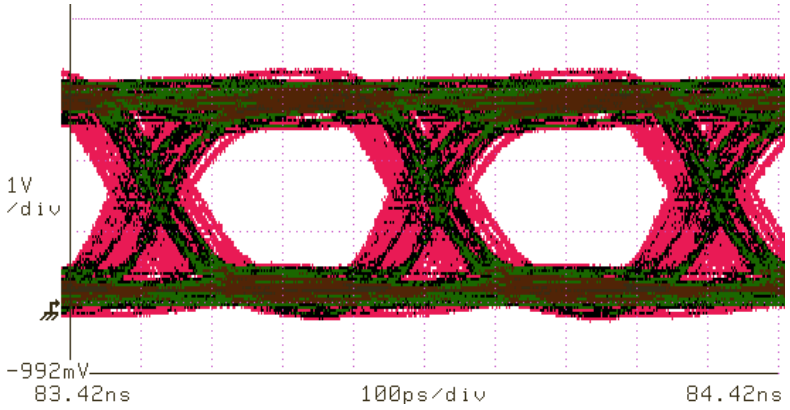
TSMC 0.35µm Chip



Bump Trenches & ACI

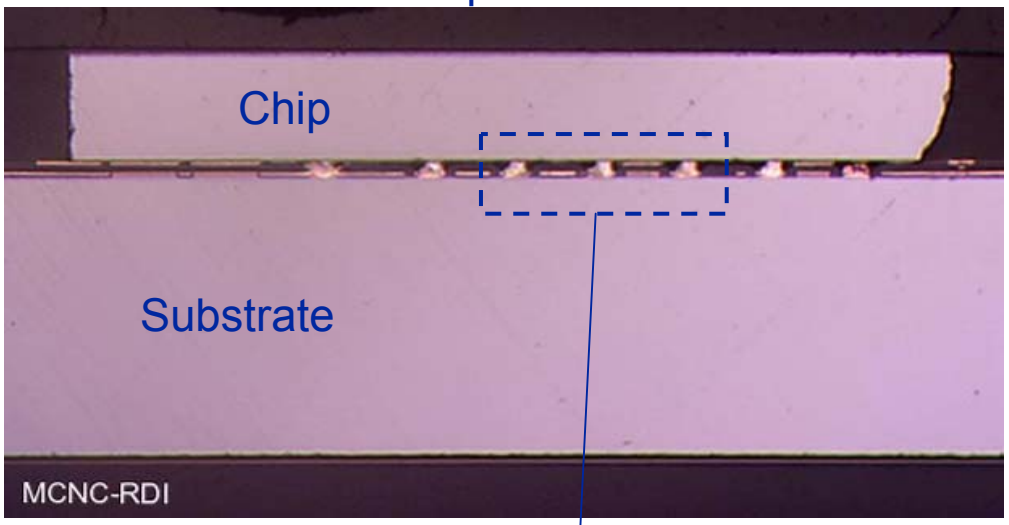
- 0.35 um CMOS Flip-chip
- 5.6cm MCM Line
- 5Gbps over two channels (2.5Gb/s/ch)



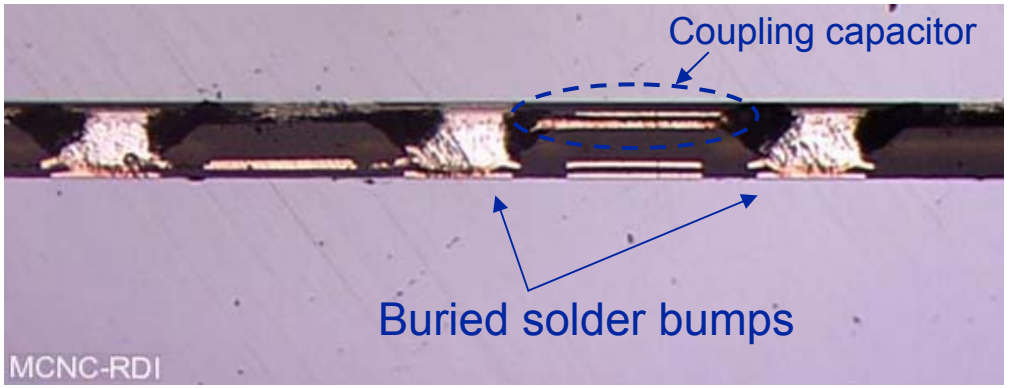


Substrate / Chip Bonding

ACCI chip and substrate



ACCI coupling capacitor and buried solder bumps



MCM-D fabricated and assembled by MCNC

Conclusions

- **AC Coupled interconnect**
  - High density reliable I/Os
  - Band-pass channel response and Equalization
- **ACCI transceiver**
  - Voltage mode driver
  - A low swing pulse receiver
- **Demonstration**
  - 15cm TL on PCB
  - MCM with 5.6cm TL on BCB substrate